Cineca HPC Infrastructure Update
March 2018
Carlo Cavazzoni

Roadmap toward exascale

Peak Performance

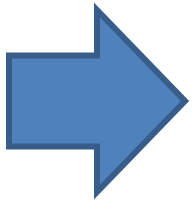
10^18 Flops

Moore law

FPU Performance

10^9 Flops

Dennard law



Number of FPUs

10^9

10^5 FPUs in 10^4 servers

10^4 FPUs in 10^5 servers

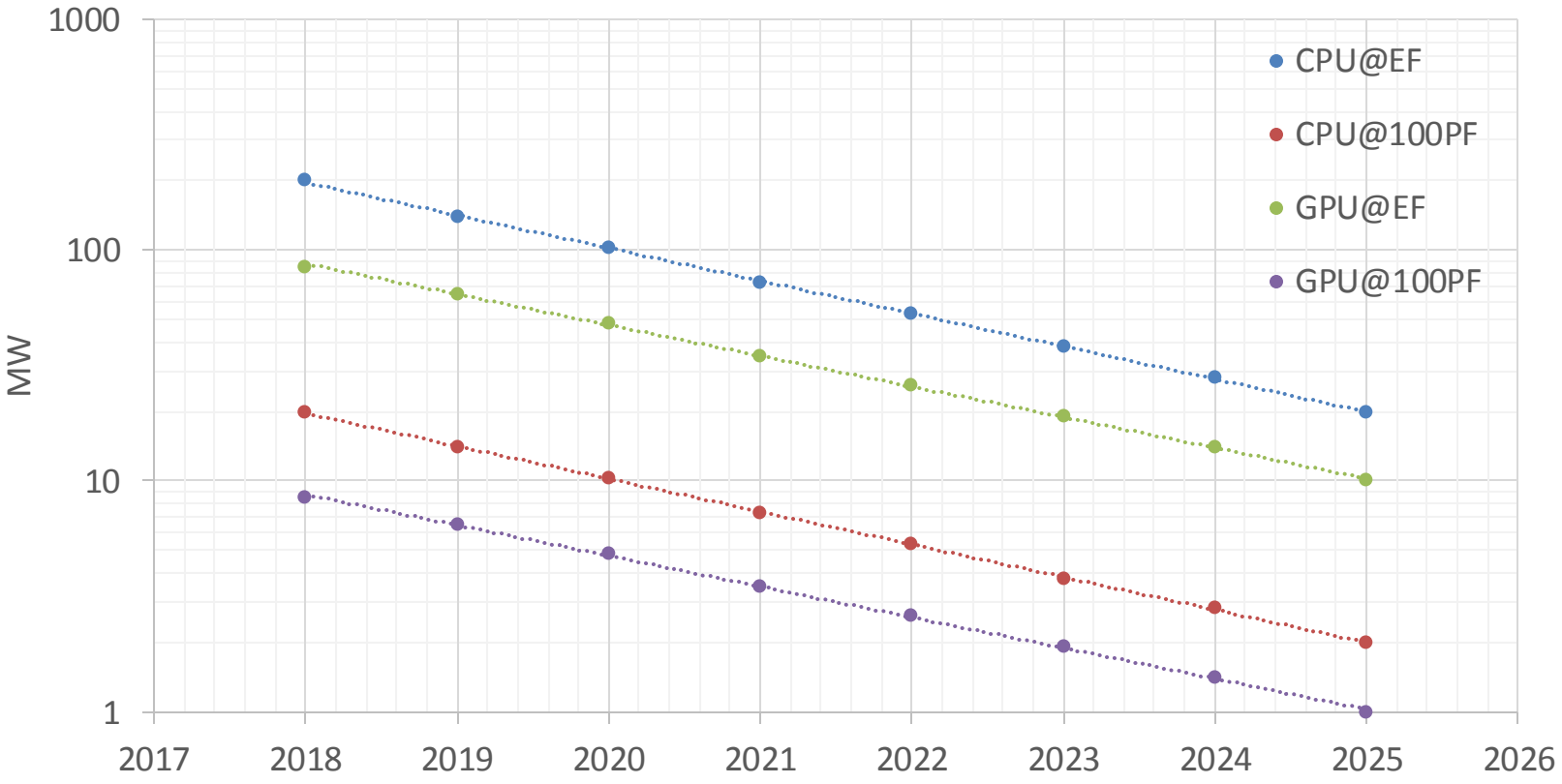
Working hypothesis

Co-design

Heterogeneus

Latency vs Throughput

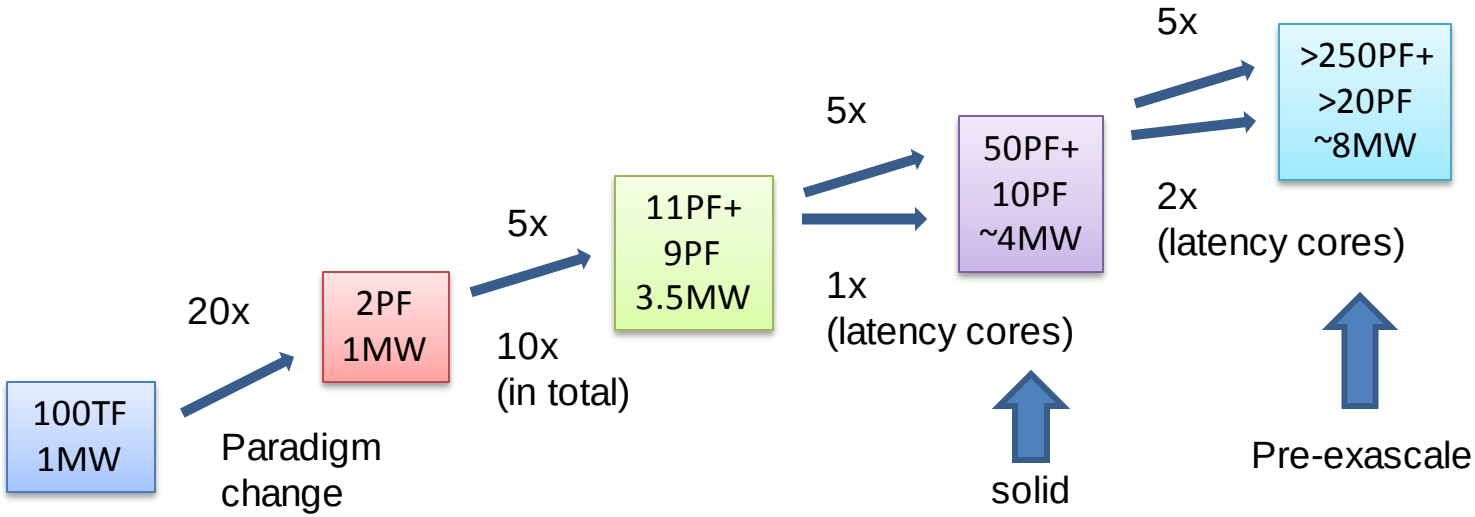
Power projection



Peek Perf (DP) @ 10MW

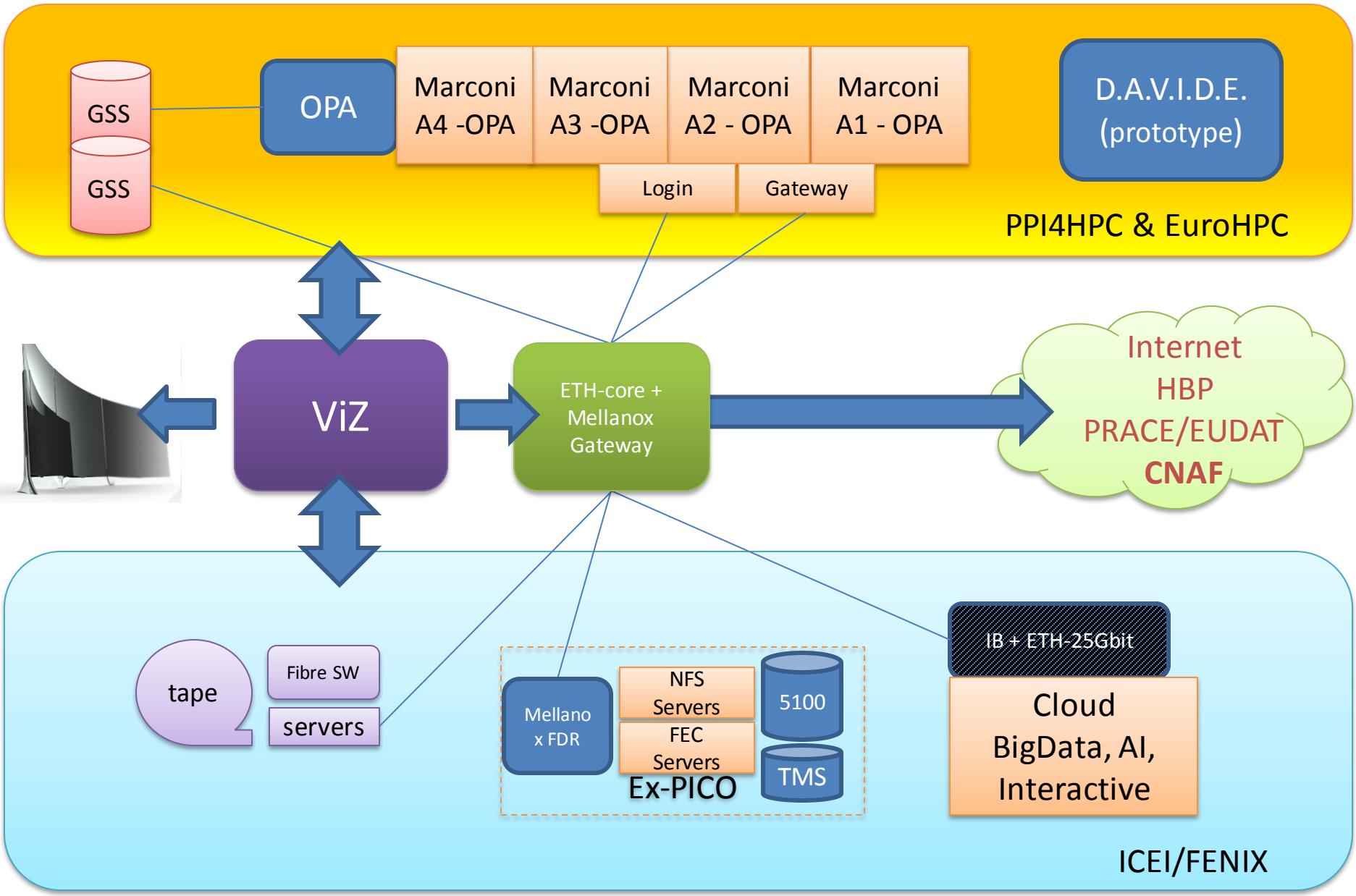
	2018	2019	2020	2021	2022	2023	2024	2025	2026
CPU	50PF	70PF	100PF	140PF	200PF	250PF	330PF	500PF	750PF
GPU	125PF	166PF	200PF	300PF	385PF	525PF	715PF	1EF	1.3EF

Cineca “sustainable” roadmap toward exascale



2009	2012/2013	2016/2017	2019/2020	2021/2022
IBM SP6 Power6	Fermi IBM BGQ PowerA2	Marconi Xeon + KNL	Marconi + PPI4HPC + ICEI (PPI-HB)	EuroHPC

New Cineca HPC infrastructure design point



HPC and Verticals